Amendments to the Specification:

In paragraph [0005]:

The MAC address table records the source MAC IDs (SIDs) of incoming packets. If there is an incoming packet to be stored in the MAC memory, a rule called "hashing" is defined for mapping the incoming packet to a specific look-up table entry based on the MAC ID of the incoming packet. Whenever a packet enters the networking apparatus, the networking apparatus picks the destination MAC ID (DID) of this incoming packet and uses the DID to perform hashing. Hashing of the DID maps this DID to a specific entry in the look-up table. The networking apparatus checks the MAC ID stored in this entry to see whether this MAC ID appeared before and has been recorded in the table, this step being called "search". If the MAC ID stored in this entry is invalid, out of date, or valid but different from the DID under searching, the search result is "missed". However, if the MAC ID stored in this entry is valid and indeed equal to the DID of the incoming packet, the search result is "hit". The networking apparatus decides how to forward the packet based on the search result. If the search result is "missed", and this packet is a legal packet, this incoming packet will be broadcasted to all the ports except the inbound port. If the search result is "hit", this incoming packet will be forwarded to the associated port. This step is called "forward". After forwarding, the network apparatus would try to "learn" the "SID-inbound port" relationship and record the relationship into the look-up table.

In paragraph [0008]:

As for ~~the~~ details concerning hashing ~~scheme~~ schemes, please refer to "a comparison of hashing schemes for address lookup in computer networks", by Jain, IEEE Transactions on Communications, COM40 (10): 1570-1573, October 1992, which is incorporated herein for reference.

In paragraph [0011]:

According to the claimed invention, a method for providing fault tolerance to memory in a networking apparatus is also disclosed. The method comprises performing a built-in self test (BIST) on a first memory when the networking apparatus powers on; marking a second memory to indicate which sections of the first memory ~~is~~ are defective; locating one of the sections of the first memory according to the packet; and checking the portion of the second memory corresponding to the located section of the first memory to determine how to handle the packet.

In paragraph [0018]:

Fig.5 is a flowchart of a packet information learning process in a networking apparatus when there is no substitute memory present according to one embodiment of the present invention.

In paragraph [0019]:

Fig.6 is a flowchart of a packet information learning process in a networking apparatus when there is a substitute memory present according to one embodiment of the present invention.

In paragraph [0030]:

Step 130: Check Status Record Memory. However, since the located entry in the SRAM 20 may be ~~detective~~ defective and therefore does not indicate which port that the packet should be forwarded to or cannot serve as the entry the

packet information should be learned into, the register 30 is checked. In this embodiment, the switch 10 checks to see how the register 30 corresponding to the located entry is marked. If the marking of the register 30 is not in a corresponding manner, the switch 10 will check if there is at least one of the markings stored in the register 30 identify the specific entry.

In paragraph [0043]:

Fig.5 is a flowchart of a packet information learning process in a networking apparatus 10 when there is no substitute memory present according to an embodiment of the present invention.

In paragraph [0047]:

Fig.6 is a flowchart of a packet information learning process in a networking apparatus 10 when there is a substitute memory present according to an embodiment of the present invention.

In paragraph [0055]:

In other words, Fig.2 to Fig.6 illustrate how a packet is handled. To be specific, Fig. 2 and Fig.3 detail packet transmission using only a SRAM 20 and set of registers 30. Fig.2 and Fig.4 also detail packet transmission but with the addition of a CAM 40. Fig.2 and Fig.5 detail packet information learning process using only a SRAM 20 and a set of registers 30. Fig.2 and Fig.6 detail packet information learning process but with the addition of a CAM 40.